What is Claimed is:

[c1] A fabrication method for integrating a plurality of heterogeneous circuit devices in a single substrate, comprising:

providing a substrate;

forming a first protective layer over the substrate;

removing a portion of the first protective layer;

ion implanting a high voltage well of a first circuit device in the substrate using the partially removed first protective layer;

forming a second protective layer over the substrate;

removing a portion of the second protective layer; and

ion implanting a first low voltage well of a second circuit device in the substrate using the partially removed second protective layer.

[c2] The method of claim 1, further comprising ion implanting a photodiode in the substrate.

[c3] The method of claim 1, further comprising forming at least one microelectomechanical system-based element in the substrate.

[c4] The method of claim 1, wherein providing a substrate comprises providing a layer of silicon.

[c5] The method of claim 4, wherein providing a layer of silicon comprises providing a layer of p-type silicon.

[c6] The method of claim 1, wherein providing a substrate comprises providing a silicon-on-insulator wafer comprising a single-crystal-silicon layer, a substrate and an insulator layer therebetween.

[c7] The method of claim 6, wherein providing a silicon-on-insulator wafer comprises providing a silicon-on-insulator wafer comprising a p-type silicon layer, a substrate and an insulator layer therebetween.

[c8] The method of claim 1, further comprising:

forming a third protective layer over the substrate;

removing a portion of the third protective layer; and

ion implanting a second low voltage well of the second circuit device in the substrate.

[c9] The method of claim 8, further comprising forming a field oxide layer over at least part of each of the high voltage well, the first low voltage well and the second low voltage well.

[c10] The method of claim 8, further comprising ion implanting the substrate to adjust a threshold of the high voltage well, the first low voltage well and the second low voltage well.

[c11] The method of claim 9, further comprising:

forming a polysilicon layer over the gate oxide and the field oxide layer; and

removing a portion of the polysilicon layer to define a polysilicon gate for each of the high voltage well, the first low voltage well and the second low voltage well.

[c12] The method of claim 11, further comprising:

forming a fourth protective layer over at least the field oxide layer and the polysilicon gates;

removing a portion of the fourth protective layer; and

ion implanting a P-body in the high voltage well of the first circuit device using the partially removed fourth protective layer.

[c13] The method of claim 12, further comprising:

forming a fifth protective layer over at least the field oxide layer and the polysilicon gates;

removing a portion of the fifth protective layer; and

ion implanting at least one N+ source/drain in the P-body, in the high voltage well and in the first low voltage well of the second circuit device using the partially removed fifth protective layer.

[c14] The method of claim 13, further comprising:

forming a sixth protective layer over at least the field oxide layer and the polysilicon gates;

removing a portion of the sixth protective layer; and

ion implanting at least one P+ source/drain in the P-body and in the second low voltage well of the second circuit device using the partially removed sixth protective layer.

[c15] The method of claim 14, further comprising forming a passivation oxide layer over at least the field oxide layer and the polysilicon gates.

[c16] The method of claim 15, further comprising:

forming a plurality of vias through the passivation oxide layer to each of the N+ and P+ sources/drains;

forming a layer of metal over the passivation oxide layer and in the vias; and

removing a portion of the layer of metal over the passivation oxide layer to define a plurality of electrical interconnects.

[c17] A heterogeneous device, comprising:

a substrate;

a high voltage well of a first circuit device defined in the substrate; and

a first low voltage device of a second circuit device defined in the substrate.

[c18] The device of claim 17, further comprising a photodiode defined in the substrate.

[c19] The device of claim 17, further comprising at least one microelectomechanical system-based element defined in the substrate.

[c20] The device of claim 17, wherein the substrate comprises a layer of silicon.

[c21] The device of claim 20, wherein the layer of silicon comprises p-type silicon.

[c22] The device of claim 17, wherein the substrate comprises a silicon-on-insulator wafer comprising a single-crystal-silicon layer, a substrate and an insulator layer therebetween.

[c23] The device of claim 22, wherein the single-crystal-silicon layer comprises p-

type silicon.

[c24] The device of claim 17, further comprising a second low voltage well of the second circuit device defined in the substrate.

[c25] The device of claim 24, further comprising a field oxide layer over at least part of each of the high voltage well, the first low voltage well and the second low voltage well.

[c26] The device of claim 25, further comprising a polysilicon gate associated with each of the high voltage well, the first low voltage well and the second low voltage well.

[c27] The device of claim 26, further comprising:

a P-body defined in the high voltage well of the first circuit device;

an N+ source/drain defined in each of the P-body, the high voltage well and the first low voltage well of the second circuit device; and

a P+ source/drain in each of the P-body and the second low voltage well of the second circuit device.

[c28] The device of claim 27, further comprising:

a passivation oxide layer over at least the field oxide layer and the polysilicon gates;

a plurality of vias through the passivation oxide layer; and

a plurality of contacts, each of the contacts extending through the vias and contacting at least one of the sources/drains.

[c29] A fabrication method for a heterogeneous device, comprising:

providing a substrate; and

successively masking, ion implanting, oxidizing, thin film depositing and annealing the substrate to define a plurality of heterogeneous circuit devices in the substrate.

[c30] The method of claim 29, further comprising forming at least one microelectromechanical system-based element in the substrate.

[c31] The method of claim 29, wherein masking the substrate comprises:

forming a protective layer; and

removing a portion of the protective layer.

[c32] The method of claim 29, wherein ion implanting the substrate to define a plurality of heterogeneous circuit devices in the substrate comprises ion implanting and annealing at least one photodiode.

[c33] The method of claim 29, wherein ion implanting the substrate to define a plurality of heterogeneous circuit devices in the substrate comprises ion implanting at least one complementary metal oxide semiconductor transistor and at least one double-diffused metal oxide semiconductor transistor.

[c34] The method of claim 33, wherein ion implanting the substrate to define a plurality of heterogeneous circuit devices in the substrate further comprises ion implanting and annealing at least one photodiode.

[c35] The method of claim 29, wherein providing a substrate comprises providing a layer of silicon.

[c36] The method of claim 35, wherein providing a layer of silicon comprises providing a layer of p-type silicon.

[c37] The method of claim 29, wherein providing a substrate comprises providing a silicon-on-insulator wafer comprising a single-crystal-silicon layer, a substrate and an insulator layer therebetween.

[c38] The method of claim 37, wherein providing a silicon-on-insulator wafer comprises providing a silicon-on-insulator wafer comprising a p-type silicon layer, a substrate and an insulator layer therebetween.

[c39] A heterogeneous device, comprising:

a substrate; and

a plurality of heterogeneous circuit devices defined in the substrate.

[c40] The device of claim 39, wherein the plurality of heterogeneous circuit devices comprises at least one complementary metal oxide semiconductor] transistor and at least one double-diffused metal oxide semiconductor] transistor.

[c41] The device of claim 39, further comprising a photodiode defined in the substrate.

[c42] The device of claim 39, further comprising at least one microelectomechanical system-based element defined in the substrate.

[c43] The device of claim 39, wherein the substrate comprises a layer of silicon.

[c44] The device of claim 43, wherein the layer of silicon comprises p-type silicon.

[c45] The device of claim 39, wherein the substrate comprises a silicon-on-insulator wafer comprising a single-crystal-silicon layer, a substrate and an insulator layer therebetween.

[c46] The device of claim 45, wherein the single-crystal-silicon layer comprises p-type silicon.